



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/824,754	04/15/2004	Dung-Ching Perng	45271.00015	7042

7590 11/16/2004
Charles E. Runyan Jr.
Squire, Sanders & Dempsey L.L.P.
Suite 300
1 Maritime Plaza
San Francisco, CA 94111

EXAMINER

RICHARDS, N DREW

ART UNIT	PAPER NUMBER
----------	--------------

2815

DATE MAILED: 11/16/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/824,754

Applicant(s)

PERNG, DUNG-CHING

Examiner

N. Drew Richards

Art Unit

2815

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 15 April 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-14 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-14 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 15 April 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-4 are rejected under 35 U.S.C. 102(b) as being anticipated by Rideout (U.S. Patent No. 4,075,045).

Rideout discloses in figures 1A-3B and on columns 1-16 an integrated circuit.

Specifically, Rideout discloses:

a substrate 2 (figure 1J);

a dielectric layer 17 disposed on the substrate and having a trench 19/20 disposed therein (figure 1I shows dielectric layer 17 with trenches 19 and 20; 19 and 20 are disclosed on column 12 line 18 as contact holes or vias, however, these contact holes or vias are considered to be "trenches" having a width approximately equal to their length, figure 2D shows a top view of trenches 19 and 20);

a conductor 21 disposed within the trench (figure 1J); and

a substantially impermeable barrier, including at least two different materials bonded together and expanded, located between the conductor 21 and the dielectric

Art Unit: 2815

layer 17 (the barrier layer is not shown but is disclosed on column 12 lines 43-49; the barrier is disclosed as being an intermetallic silicide such as platinum silicide or palladium silicide such that the barrier includes at least two different materials bonded together, i.e. either platinum and silicon or palladium and silicon; the silicides are considered to be "expanded" as the final silicide layer will have a thickness greater than that of either the platinum/palladium or the silicon layer alone; the barrier of Rideout is considered to be "substantially impermeable" in so much as Rideout teaches the same materials as claimed).

With regard to claim 2, one of the materials includes palladium.

With regard to claim 3, one of the materials includes platinum.

With regard to claim 4, the barrier further includes silicon.

3. Claims 1-6 are rejected under 35 U.S.C. 102(e) as being anticipated by Lopatin (U.S. Patent No. 6,420,189 B1).

Lopatin discloses in figures 1-15 and on columns 1-16 an integrated circuit.

Specifically, Lopatin discloses:

a substrate (though a substrate is not specifically shown in figures 1-13, first damascene channel 102 as seen in figure 7 is considered part of the substrate, first damascene channel 102 is disclosed as being formed over active circuit elements and a dielectric on an integrated chip and thus a substrate is implicitly disclosed, column 6 lines 27-31);

Art Unit: 2815

a dielectric layer 114/110 disposed on the substrate and having a trench 108 disposed therein (figure 7);

a conductor 124 disposed within the trench 108 (figure 7); and

a substantially impermeable barrier 120/122, including at least two different materials bonded together and expanded, located between the conductor 124 and the dielectric layer 114/110 (the first portion of the barrier 120 is disclosed on column 6 lines 52-59 as being a variety of materials such as TaN, TaSiN, TiSiN, TiW, or alloys such as NiW, NiTa, PdW, PdTa and PdMo; the second portion of the barrier 122 is disclosed on column 9 lines 44-52 as being a variety of materials such as gold, palladium, platinum or alloys thereof; thus both portions 120/122 of the barrier are disclosed to include at least two different materials bonded together; the compounds and alloys disclosed are considered to be "expanded" as the final layer will have a thickness greater than that of either of the single materials alone; the barrier of Lopatin is considered to be "substantially impermeable" in so much as Lopatin teaches the same materials as claimed).

With regard to claim 2, one of the materials includes palladium (column 9 lines 50-52).

With regard to claim 3, one of the materials includes platinum (column 9 lines 50-52).

With regard to claim 4, the barrier further includes silicon (column 6 line 54, TaSiN or TiSiN include silicon).

Art Unit: 2815

With regard to claim 5, the conductor 124 includes copper (124 is disclosed as Y-Ba-Cu on column 10 line 11).

With regard to claim 6, the barrier 120/122 has a thickness between about 2 nm to about 200 nm (see column 9 lines 39-42 and 65-67).

4. Claims 7, 8, 10, 13 and 14 are rejected under 35 U.S.C. 102(b) as being anticipated by Dubin et al. (U.S. Patent No. 5,695,810).

Dubin et al. disclose in figures 1-10 and on columns 1-10 an integrated circuit. Specifically, Dubin et al. disclose:

a conductor 16 disposed on a substrate 9 (figure 5); and

a substantially impermeable barrier 15/17 encapsulating at least a top surface and side surface of the conductor 16 (figure 5; the barrier of Dubin et al. is considered to be "substantially impermeable" in so much as Dubin et al. teach the same materials as claimed).

With regard to claim 8, Dubin et al. further disclose an insulator 11 adjacent to at least a portion of the barrier 15/17 (figure 5).

With regard to claim 10, the barrier includes CoWP (column 5 lines 66-67 and column 7 line 42).

With regard to claim 13, the conductor includes copper (column 6 lines 35-37).

With regard to claim 14, the substantially impermeable barrier 15/17 also encapsulates at least a portion of a bottom surface of the conductor 16 (figure 5).

Art Unit: 2815

5. Claims 7-9 and 11-14 are rejected under 35 U.S.C. 102(e) as being anticipated by Leu et al. (U.S. Patent No. 6,605,874 B2).

Leu et al. disclose in figures 1A-9 and on columns 1-20 an integrated circuit.

Specifically, Leu et al. disclose:

a conductor 112 disposed on a substrate 110 (figure 1A); and

a substantially impermeable barrier 134/114 encapsulating at least a top surface and side surface of the conductor 112 (figure 1A; the barrier of Leu et al. is considered to be "substantially impermeable" in so much as Leu et al. teach the same materials as claimed; also Leu et al. teach the barrier being a diffusion barrier for copper, column 2 lines 55-56).

With regard to claim 8, Leu et al. further disclose an insulator 126 adjacent to at least a portion of the barrier 134/114 (figure 1A).

With regard to claim 9, the barrier includes CoWB (column 9 line 8).

With regard to claim 11, the barrier includes COWB(p) (column 9 line 8, COWBP is considered to be the same material).

With regard to claim 12, the barrier has a thickness between about 2 nm to about 200 nm (column 3 lines 61-65).

With regard to claim 13, the conductor includes copper (column 2 line 66, "the interconnect structures comprising copper").

With regard to claim 14, the substantially impermeable barrier 134/114 also encapsulates at least a portion of a bottom surface of the conductor 112 (figure 1A).

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Lee et al. (U.S. Patent No. 6,436,816 B1).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to N. Drew Richards whose telephone number is (571) 272-1736. The examiner can normally be reached on Monday-Friday 9:00-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (571) 272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



N. Drew Richards
AU 2815